Subject Name: MPMC
Prepared by (Faculty (s) Name): Y.JALAJAKSHI

Year and Sem, Department:III& II SEM, ECE

Unit – I: 8086 Architecture

Important Points / Definitions:

- 8086 Microprocessor is an enhanced version of 8085Microprocessor that was designed by Intel in 1976.
- It is a 16-bit Microprocessor having 20 address lines and16 data lines that provides up to 1MB storage.
- It consists of powerful instruction set, which provides operations like multiplication and division easily.
- It supports two modes of operation, i.e. Maximum mode and Minimum mode. Maximum mode is suitable for system having multiple processors and Minimum mode is suitable for system having a single processor.
- It has an instruction queue, which is capable of storing six instruction bytes from the memory resulting in faster processing.
- It was the first 16-bit processor having 16-bit ALU, 16-bit registers, internal data bus, and 16-bit external data bus resulting in faster processing.
- It is available in 3 versions based on the frequency of operation −
    - 8086 → 5MHz
    - 8086-2 → 8MHz
    - (c)8086-1 → 10 MHz
- It uses two stages of pipelining, i.e. Fetch Stage and Execute Stage, which improves performance.
- Fetch stage can prefetch up to 6 bytes of instructions and stores them in the queue.
- Execute stage executes these instructions.
- It has 256 vectored interrupts.
- It consists of 29,000 transistors.

8086 Microprocessor is divided into two functional units, i.e., **EU** (Execution Unit) and **BIU** (Bus Interface Unit).

- Execution unit gives instructions to BIU stating from where to fetch the data and then decode and execute those instructions. Its function is to control operations on data using the instruction

decoder & ALU. EU has no direct connection with system buses as shown in the above figure, it performs operations over data through BIU.

- ALU handles all arithmetic and logical operations, like +, −, ×, /, OR, AND, NOT operations.
- Flag Register is a 16-bit register that behaves like a flip-flop, i.e. it changes its status according to the result stored in the accumulator. It has 9 flags and they are divided into 2 groups − Conditional Flags and Control Flags.
- BIU takes care of all data and addresses transfers on the buses for the EU like sending addresses, fetching instructions from the memory, reading data from the ports and the memory as well as writing data to the ports and the memory. EU has no direction connection with System Buses so this is possible with the BIU. EU and BIU are connected with the Internal Bus.
- **Instruction queue** − BIU contains the instruction queue. BIU gets up to 6 bytes of next instructions and stores them in the instruction queue. When EU executes instructions and is ready for its next instruction, then it simply reads the instruction from this instruction queue resulting in increased execution speed.
- Fetching the next instruction while the current instruction executes is called **pipelining**.
- **Segment register** − BIU has 4 segment buses, i.e. CS, DS, SS& ES. It holds the addresses of instructions and data in memory, which are used by the processor to access memory locations. It also contains 1 pointer register IP, which holds the address of the next instruction to execute by the EU.
- **Instruction pointer** − It is a 16-bit register used to hold the address of the next instruction to be executed.
- 8086 was the first 16-bit microprocessor available in 40-pin DIP (Dual Inline Package) chip.

SHORT QUESTIONS:

1. How many instructions can be executed per second in 8086/8088?
2. What are the features of Intel 8086?
3. What is Logical Address?
4. What is Effective Address?
5. What is data and address size in 8086?
6. Explain the function of M/IO in 8086?
7. Explain the functions of EU and BIU
8. What is the size of instruction queue in 8086?
9. What are the Interrupts of 8086?
10. What is the position of stack pointer after the PUSH and POP instruction?
11. How is the clock signal generated in 8086?
12. What is PSW? Give Its Structure?
13. Draw the timing diagram

14. What is Effective Address? ...
15. What is data and address size in 8086?

LONG QUESTIONS:

1) Draw the register organization of 8086 Microprocessor and explain it.
2) Explain the minimum mode pins of 8086 Microprocessor in detail.
3) Explain the concept of physical address calculation of 8086 microprocessor
4) Draw the internal architecture of 8086 microprocessor and explain its operation.
5) Draw the timing diagram of minimum mode write operation and explain it.
6) Define addressing mode and explain different addressing modes used in 8086 Microprocessor with examples.
7) List out different assembler directives used in 8086 microprocessor with examples.
8) List the string manipulation instruction set of 8086 microprocessor with example.

Fill in the blanks / choose the Best:

1. _____ signal is generated by combining RD and WR signals with IO
   A. control
   B. memory
   C. register
   D. system

2. The intel 8086 microprocessor is a _____ processor
   A. 8 bit
   B. 16 bit
   C. 32 bit
   D. 4 bit

3. In 8086 microprocessor , the address bus is _____ bit wide
   A. 12 bit
   B. 10 bit
   C. 16 bit
   D. 20 bit

4. The work of EU is _____
   A. encoding
   B. decoding
   C. processing

   D. D. calculations

5. The 16 bit flag of 8086 microprocessor is responsible to indicate _____
   A. the condition of result of ALU operation
   B. the condition of memory
   C. the result of addition
   D. the result of subtraction

6. The OF is called as _____
   A. overflow flag
   B. overdue flag
   C. one flag
   D. over flag

7. The BP is indicated by _____
   A. base pointer
   B. binary pointer
   C. bit pointer
   D. digital pointer

8. The index register are used to hold _____
   A. memory register
   B. offset address
   C. segment memory
   D. offset memory

9. The BIU contains FIFO register of size _____ bytes
   A. 8
   B. 6
   C. 4
   D. 12

10. The 1 MB byte of memory can be divided into _____ segment
    A. 1 Kbyte
    B. 64 Kbyte
    C. 33 Kbyte
    D. 34 Kbyte

11. _____ is used to write into memory
    A. RD
    B. WR
    C. RD / WR
    D. CLK

12. The RD, WR, M/IO is the heart of control for a _____ mode
A. minimum
B. maximum
C. compatibility mode
D. control mode

13. If MN/MX is low the 8086 operates in _____ mode
A. Minimum
B. Maximum
C. both (A) and (B)
D. medium

14. In max mode, control bus signal So,S1 and S2 are sent out in _____ form
A. decoded
B. encoded
C. shared
D. unshared

15. The ___ bus controller device decodes the signals to produce the control bus signal
A. internal
B. data
C. external
D. address

Instruction Set and Assembly Language Programming of 8086

Important Points / Definitions:

- The Addressing modes in the 8086 are classified as register, immediate, data memory, stack memory and program memory addressing modes

- The data memory addressing modes are classified as Direct, Base, index, Base plus indexed, base-relative, index-relative and base-relative plus index addressing modes

- The program memory addressing modes are classified as direct, relative and indirect addressing modes

- The 8086 instructions are classified as data transfer, arithmetic, logical, shift/rotate, flag control, control transfer, string and machine control instructions

- Assembler directives are used while writing an assembly language program that is to be assembled by an assembler

Questions:

1. Which Registers are modified while executing inter segment and intra segment jump instructions?

2. Is it possible to exchange the contents of two memory locations or the content of two segment registers using XCHG instruction? Why?

3. If the content of BP=1000H and SI=2000h, What is the value present in CX after the 8086 executes the instructions LEA CX, [BP+SI] and LEA CX, [SI]

4. Is it possible to use two memory operands in the ADD and SUB instructions?
5. What is the difference between SUB and CMP instructions?

6. Is the carry flag affected by the execution of INC and DEC instruction? Why?

7. What is the difference between TEST and AND instructions?

8. What are the common applications of left shift and right shift operations?
9. What is the difference between Arithmetic and logical right shift?

10. What is the function of Assembler and Assembler directives?

Fill in the blanks / choose the Best:

1. In which of these modes, the immediate operand is included in the instruction itself?

a) register operand mode
b)immediate operand mode
c)register and immediate operand mode

d) none of the mentioned

2. In register address mode, the operand is stored in

a) 8-bit general purpose register
b) 16-bit general purpose register
c) si or di
d)all of the mentioned

3. In which of the following addressing mode, the offset is obtained by adding displacement and contents of one of the base registers?

a) direct mode
b) register mode
c) based mode
d) indexed mode

4. In which of the following addressing mode, the offset is obtained by adding displacement, with the contents of SI?
a) direct mode b) register
mode c) based mode
d) indexed mode

5. The address of location of operand is calculated by adding the contents of any of the base registers, with the contents of any of index registers in
a) based indexed mode with displacement
b) based indexed mode
c) based mode
d) indexed mode

6. Which of the following is not a data type of 80286?
a) Ordinal or unsigned
b) ASCII
c) Packed BCD
d) None of the mentioned

7. The representation of 8-bit or 16-bit signed binary operands using 2"s complement is a data type of
a) Ordinal
b) ASCII
c) Packed BCD
d) integer

8. The instruction that multiplies the content of AL with a signed immediate operand is

a) MUL
b) SMUL
c) IMUL
d) None of the mentioned

9. The instruction that represents the „rotate source, count" is
a) RCL
b) RCR
c) ROR
d) All of the mentioned

10. The instruction that is used to transfer the data from source operand to destination operand is
a) data copy/transfer instruction
b) branch instruction
c) arithmetic/logical instruction
d) string instruction

11. Which of the following is not a data copy/transfer instruction?
a) MOV
b) PUSH
c) DAS
d) POP

12. The instructions that involve various string manipulation operations are
a) branch instructions
b) flag manipulation instructions
c) shift and rotate instructions
d) string instructions

13. Which of the following instruction is not valid?
a) MOV AX, BX
b) MOV DS, 5000H
c) MOV AX, 5000H
d) PUSH AX

14. In PUSH instruction, after each execution of the instruction, the stack pointer is
a) incremented by 1
b) decremented by 1
c) incremented by 2
d) decremented by 2

15. The instruction that pushes the contents of the specified register/memory location on to the stack

is
a) PUSHF
b) POPF
c) PUSH
d) POP

16. In POP instruction, after each execution of the instruction, the stack pointer is
a) incremented by 1
b) decremented by 1
c) incremented by 2
d) decremented by 2

17. The instructions that are used for reading an input port and writing an output port respectively are
a) MOV, XCHG
b) MOV, IN
c) IN, MOV
d) IN, OUT

18. The instruction that is used for finding out the codes in case of code conversion problems is
a) XCHG
b) XLAT
c) XOR
d) JCXZ

19. The instruction that loads effective address formed by destination operand into the specified source register is
a) LEA
b) LDS
c) LES
d) LAHF

20. The instruction that loads the AH register with the lower byte of the flag register is
a) SAHF
b) AH
c) LAHF
d) PUSHF

21. The instruction that pushes the flag register on to the stack is a)
PUSH
b) POP
c) PUSHF d) POPF

Unit –II: Introduction to Microcontrollers

Important Points / Definitions:

- 8051 microcontroller is designed by Intel in 1981. It is an 8-bit microcontroller.
- It is built with 40 pins DIP (dual inline package), 4kb of ROM storage and 128 bytes of RAM storage, 2 16-bit timers.
- It consists of are four parallel 8-bit ports, which are programmable as well as addressable as per the requirement.
- An on-chip crystal oscillator is integrated in the microcontroller having crystal frequency of 12 MHz.
- The system bus connects all the support devices to the CPU. The system bus consists of an 8-bit data bus, a 16-bit address bus and bus control signals.
- All other devices like program memory, ports, data memory, serial interface, interrupt control, timers, and the CPU are all interfaced together through the system bus.

The pin diagram of 8051 microcontroller looks as follows

1. **Pins 1 to 8** − These pins are known as Port 1. This port doesn‟t serve any other functions. It is internally pulled up, bi-directional I/O port.
2. **Pin 9** − It is a RESET pin, which is used to reset the microcontroller to its initial values.
3. **Pins 10 to 17** − These pins are known as Port 3. This port serves some functions like interrupts, timer input, control signals, serial communication signals RxD and TxD, etc.
4. **Pins 18 & 19** − These pins are used for interfacing an external crystal to get the system clock.
5. **Pin 20** − This pin provides the power supply to the circuit.
6. **Pins 21 to 28** − These pins are known as Port 2. It serves as I/O port. Higher order address bus signals are also multiplexed using this port.
7. **Pin 29** − This is PSEN pin which stands for Program Store Enable. It is used to read a signal from the external program memory.
8. **Pin 30** − This is EA pin which stands for External Access input. It is used to enable/disable the external memory interfacing.
9. **Pin 31** − This is ALE pin which stands for Address Latch Enable. It is used to demultiplex the address-data signal of port.
10. **Pins 32 to 39** − These pins are known as Port 0. It serves as I/O port. Lower order address and data bus signals are multiplexed using this port.
11. **Pin 40** − This pin is used to provide power supply to the circuit.

Questions

1. Discuss the advantages of microcontrollers over microprocessors in control applications?
2. Discuss the criteria for selecting a microcontroller device
3. List few features of 8051 microcontroller?
4. Discuss the advantages and disadvantages of Harvard and Von Neuman architectures.
5. What is the purpose of ALU ?
6. Name 2 register that consists of 16 bit.
7. What are SFR?
8. Draw the memory organisation of mcs – 51.
9. What are all addressing modes of mcs-51?
10. Enlist the various flags in the PSW register.
11. Discuss interfacing of external 16K EPROM and 8K RAM with the microcontroller.
12. Define and describe the directives of 8051 Microcontroller.
13. Explain classification of instruction used for 8051 microcontroller.

Fill in the blanks / choose the Best:

1.In the bit-addressable RAM of 8051, among the byte addresses 99H and 89H

A. Both are bit-addressable
B. Only 99H is bit-addressable
C. Only 89H is bit-addressable
D. None is bit-addressable

2.If RS0 = 0 and RS1 = 1, the register bank address range is
A. 00H-07H
B. 08H-0FH
C. 10H-17H
D. 18H-1FH

3.The number of timers in an 8051 microcontroller is
A. 2
B. 5
C. 1
D. 0

4.The size of On-Chip ROM in an 8051 microcontroller is
A. 4k Bytes
B. 8k Bytes
C. 16k Bytes
D. 32k Bytes

5.The width of the Program Counter in an 8051 microcontroller is
A. 8 bits
B. 16 bits
C. 32 bits
D. None of the given options

6.Which of the following pins is the external data memory write strobe in 8051?
A. P3.4
B. P3.5
C. P3.6
D. P3.7

7.To get input from a port bit of 8051 if a '1' is not written to it, reading of which value may create problem?
A. 0
B. 1
C. Both 1 and 0
D. None of 1 or 0

8.Which of the following statements is TRUE with respect to an 8051 microcontroller?
A. The SFR address of the register PSW is 0E0H
B. The SFR TMOD is a bit-addressable one
C. The SFR P2 corresponds to the Port 3 of the microcontroller
D. The SFR instruction MOV P1, A is same as MOV 90H, A

9.If CY = 1, A = 95H, and B = 4FH prior to the execution of "SUBB A, B", what will be the contents of A after the subtraction?

A. 46H
B. 45H
C. BAH
D. B9H

10.How many times the „RL" instruction needs to be executed, in order to mimic the „SWAP" instruction in an 8051 microcontroller?

A. 24
B. 26
C. 28
D. 30

11.What can one infer from the instruction „MOV TMOD, #02H" in an 8051 microcontroller?

A. Set Timer 1 in 13-bit timer operating mode
B. Set Timer 0 in 13-bit timer operating mode
C. Set Timer 1 in 8-bit auto reload timer mode
D. Set Timer 0 in 8-bit auto reload timer mode

12.In an 8051 microcontroller, it is required to configure the least significant four bits of port P0 as input. The statement for this is

A. MOV P0, #0FH
B. MOV P0, 0FH
C. MOV P0, #F0H
D. MOV P0, F0H

13.Which of the following flags are affected by the instruction „DIV AB" of an 8051 microcontroller?

A. OV, CY, AC
B. OV, AC
C. OV, CY
D. CY, AC

14.What will be the address of the memory location whose contents will be present in the Accumulator after the following set of instructions are executed?

MOV DPTR, #2004H
MOV A.,#4
MOVC A, @A + DPTR

A. 2008H
B. 2000H
C. 20H
D. 04H

15.Which of the following option is true if the following set of instructions is executed separately?
Instruction 1: MOVX @DPTR,A
Instruction 2: MOVX @R0,A

A. For Instruction 1, Accumulator is moved to the 16-bit External Memory address. For Instruction 2, Accumulator is moved to the 16-bit External Memory address.

B. For Instruction 1, Accumulator is moved to the 8-bit External Memory address. For Instruction 2, Accumulator is moved to the 16-bit External Memory address.
C. For Instruction 1, Accumulator is moved to the 8-bit External Memory address. For Instruction 2, Accumulator is moved to the 8-bit External Memory address.
D. For Instruction 1, Accumulator is moved to the 16-bit External Memory address. For Instruction 2, Accumulator is moved to the 8-bit External Memory address.

16. What is the value of the bits 4-7 of R0 after the following set of instructions are executed?
MOV @R0, #04H
MOV A, #11H
XCHD A, @R0
A. 0H
B. 4H
C. 5H
D. 1H

8051 Real Time Control

Important Points / Definitions:

- Interrupts are the events that temporarily suspend the main program, pass the control to the external sources and execute their task. It then passes the control to the main program where it had left off.

- 8051 has 5 interrupt signals, i.e. INT0, TFO, INT1, TF1, RI/TI. Each interrupt can be enabled or disabled by setting bits of the IE register and the whole interrupt system can be disabled by clearing the EA bit of the same register.

- IE(Interrupt Enable) Register is responsible for enabling and disabling the interrupt. EA register is set to one for enabling interrupts and set to 0 for disabling the interrupts.

- IP (Interrupt Priority) Register

- IP (Interrupt Priority) Register is used to change the priority levels of the interrupts by changing the corresponding bit in the Interrupt Priority (IP) register

- TCON register specifies the type of external interrupt to the microcontroller.

- 8051 has two 16-bit programmable UP timers/counters. They can be configured to operate either as timers or as event counters. The names of the two counters are T0 and T1 respectively. The timer content is available in four 8-bit special function registers, TL0,TH0,TL1 and TH1 respectively.

- In the "timer" function mode, the counter is incremented in every machine cycle. Thus, one can think of it as counting machine cycles. Hence the clock rate is 1/12 th of the oscillator frequency.

- In the "counter" function mode, the register is incremented in response to a 1 to 0 transition at its corresponding external input pin (T0 or T1). It requires 2 machine cycles to detect a high to low transition. Hence maximum count rate is 1/24 th of oscillator frequency.

- The operation of the timers/counters is controlled by two special function registers, TMOD and TCON respectively.

- TMOD register is not bit addressable

- TMOD Address: 89

- Various bits of TMOD are described as follows –

- Gate: This is an OR Gate enabled bit which controls the effect of $\overline{INT1/0}$ on START/STOP of Timer. It is set to one ('1') by the program to enable the interrupt to start/stop the timer. If

  TR1/0 in TCON is set and signal on $\overline{INT1/0}$ pin is high then the timer starts counting using either internal clock (timer mode) or external pulses (counter mode).

- M1 and M0 are mode select bits used to define Timers in different modes.

- The serial port of 8051 is full duplex, i.e., it can transmit and receive simultaneously.

- The register SBUF is used to hold the data. The special function register SBUF is physically two registers. One is, write-only and is used to hold data to be transmitted out of the 8051 via TXD. The other is, read-only and holds the received data from external sources via RXD.

- Both mutually exclusive registers have the same address 099H.

- Serial Port Control Register (SCON)

- Register SCON controls serial data communication. Address: 098H (Bit addressable)

SHORT QUESTIONS:

1. Explain different modes of Timer for 8051 microcontroller

2. List the interrupts available in the 8051 microcontroller. Explain interrupt enable (IE) SFR and Interrupt priority (IP) SFR.

3. Explain TCON and TMOD SFR for 8051 Microcontroller.

4. Explain different mode for serial communication for 8051 Microcontroller.

5. Explain operation of timer in mode 1. Discuss programming steps to generate time delay using mode 1 Write program to generate delay of 1 second using timer 0 in mode 1.

6. Write a program to transfer the message “YES” serially do this continuously. Write an 8051 program to generate 5 KHz pulse waveform of 50% duty cycle on pin 1.0 using timer-1 in mode-2.

7. Write and explain bit format for SCON and PCON SFR for 8051 Microcontroller

8. Write an ALP to sort block of ten data stored in external memory location from 4000h in ascending order.

9. Write an 8051 program count number of 0"s in data stored in 60 h memory location

10. Write an 8051 program count number of 1"s in data stored in 50 h memory location.

LONG QUESTIONS:

1. Write an 8051 program to add 16 bit data stored in external memory location starting from 5000H to 5003H. Store answer at external memory location 6000 and 6001H.
2. Write a program to send the text string "hello" to serial port 1. Set the baud rate at 9600, 8 bit data, and 1 stop bit.
3. Draw and explain mode 2 for timer of 8051 controller. Write a program to generate square wave of frequency 5Kz on pin 1.4.
4. List out the different instruction set of 8051 microcontroller and explain with examples. b) Write an assemble language program for LED blinking in 8051 microcontroller
5. Explain the different futures of 8051 microcontroller in detail
6. Draw the internal architecture of 8051 Microcontroller and explain its operation.
7. Explain how interrupts are handled in 8051
8. Write notes on 8051 serial port programming.
9. Draw the Internal RAM memory organization in 8051.
10. Explain the I/O pins ports and circuit details of 8051 with its diagram.

Fill in the blanks / choose the Best:

1. In idle mode of power control register, which of the following is not true?
   A. All of registers , ports and internal RAM maintain their data
   B. The ALE and PSEN output are held low
   C. The internal CPU clock is gated off
   D. Interrupt, Timer, and Serial Port functions act normally
2. In power down mode of power control register which of the following is not true?
   A. All functions are stopped, the contents of the on-chip RAM and Special Function Registers are lost

B. The ALE and PSEN output are held low
C. Last instruction executed before going into the power down mode
D. The on-chip oscillator is stopped

3. In Serial control (SCON) Register, SCON.5 is used to
   A. Transmit interrupt flag
   B. Receive interrupt flag
   C. Used for multi processor communication
   D. Receive enable

4. In serial communication which of the following mode of operation receives/transmits 10 bits?
   A. Mode 0
   B. Mode 1
   C. Mode 2
   D. Mode 3
5. In Timer Control Register, Mode 1 uses
   A. 8-bit timer
   B. 16-bit timer
   C. 13-bit timer
   D. 32-bit timer
6. In which of the following cases, TF0 will be „1"
   A. TH0 – TL0 = FFFDH
   B. TH0 – TL0 = FFFEH
   C. TH0 – TL0 = FFFFH
   D. TH0 – TL0 = 0000H
7. The following program generates a square wave on pin P1.5 Using timer 1. Find the frequency. Consider XTAL = 11.0592 MHz.

```
        MOV TMOD ,#10H AGAIN: MOV
        TL1, #26H
        MOV TH1, #71H
        SETB TR1
BACK: JNB   TF1,BACK
        CLR   TR1
        CPL   P1.5
        CLR TF1
        SJMP AGAIN
```

   A. 12.087 Hz
   B. 12.601 Hz
   C. 13.052Hz
   D. 14.705 Hz

8. Assuming XTAL = 11.0592 MHz, which of the following program will generate a square wave of 100 Hz frequency on pin P2.3.

A.
```
MOV  TMOD,#10H
AGAIN:   MOV  TL1,#00H
         MOV  TH1,#DCH
         SETB TR1
BACK: JNB  TF1,BACK
         CLR  TR1
         CPL  P2.3
         CLR  TF1
         SJMP AGAIN
```

B.
```
MOV  TMOD,#10H
AGAIN:   MOV  TL1,#00H
         MOV  TH1,#DEH
         SETB TR1
              BAC
BACK: JNB  TF1,   K
         CLR  TR1
         CPL  P2.3
         CLR  TF1
         SJMP AGAIN
```

C.
```
MOV  TMOD,#10H
AGAIN:   MOV  TL1,   #00H
                     #EE
         MOV  TH1,   H
         SETB TR1
BACK: JNB  TF1,   BACK
         CLR  TR1
         CPL  P2.3
         CLR  TF1
         SJMP
         AGAIN
```

D.
```
MOV  TMOD,#10H
AGAIN:   MOV  TL1,#FFH
         MOV  TH1,#EEH
         SETB TR1
BACK: JNB  TF1,   BACK
         CLR  TR1
         CPL  P2.3
         CLR  TF1
         SJMP AGAIN
```

9. What is the default interrupt priority in 8051?
   A. INT0 > TF0 > RI + TI > INT1 > TF1
   B. INT1 > TF1 > RI + TI > INT0 > TF0
   C. INT0 > TF0 > INT1 > TF1 > RI + TI
   D. INT1 > TF1 > INT0 > TF0 > RI + TI

10. Which of the following statements is true?
    A. In Simplex mode of serial communication, data is transmitted both from the transmitter to the receiver, as well as from the receiver to the transmitter
    B. In Half Duplex mode of serial communication, data is transmitted only from the transmitter to the receiver
    C. In Full Duplex mode of serial communication, data is exchanged between the transmitter and the receiver using two different channels
    D. None of the options mentioned
11. For an 8051 microcontroller, what is the combination of the START and STOP bits while performing a serial communication operation?
    A. START – Low, STOP – Low
    B. START – Low, STOP – High
    C. START – High, STOP – Low
    D. START – High, STOP – High
12. Which pins of an 8051 microcontroller function as the RxD and TxD pins during a serial communication operation?
    A. TxD – P3.1, RxD – P3.0
    B. TxD – P3.0, RxD – P3.1
    C. TxD – P3.0, RxD – P3.0
    D. TxD – P3.1, RxD – P3.1
13. What are the contents of the SBUF register, after executing the following instruction? MOV SBUF, #'A'
    A. 41H
    B. 40H
    C. 42H
    D. 39H
14. Which register in an 8051 microcontroller contains the SMOD bit?
    A. SBUF
    B. TMOD
    C. PCON
    D. TCON

15. Which bits in the PCON register of an 8051 microcontroller correspond to the idle and power-down modes?
    A. PCON.0 – Idle mode, PCON.1 – Power-down mode
    B. PCON.1 – Idle mode, PCON.0 – Power-down mode
    C. PCON.0 – Idle mode/Power-down mode
    D. PCON.1 – Idle mode/Power-down mode

Unit – III : I/O Interface, Interfacing with Advanced Devices, Communication interface

Important Points / Definitions:

I/O interface

- All I/O peripherals that are covered in this course are 8-bit so they have to be interfaced only to D0-D7 or D8-D15 - not to both the buses.
- If I/O device is connected to D0-D7 then only even addresses must be assigned.
- If I/O device is connected to D8-D15 then only odd addresses must be assigned.
- When using fixed addressing - then it is suffice to use Address lines A0-A7 for decoding and addressing.
- When using variable addressing - then you need to use Address lines A0-A15 for decoding and addressing.
- With I/O mapped I/O IOR and IOW should be used for read and write.
- If memory mapped I/O use MEMR and MEMW.
- In case of memory mapped I/O you need to ensure that there is no clash between memory and I/O address - for eg. address 01000H should not be assigned to both memory and I/O devices

Interfacing with Advanced Devices

- Hardware Interrupt: It is an interrupt generated by activating the interrupt pin of 8086
- Interrupt Vector: It is a four byte in the Interrupt Vector Table, which contains a 16-bit offset part and a 16-bit segment part that are loaded in the IP and CS registers respectively when an interrupt is received
- Interrupt Vector Table: It is a table in the memory which contains the interrupt vectors of the different interrupts
- INTR: It is a maskable hardware interrupt in the 8086 that can be enabled and disabled using Interrupt flag
- Non Maskable Interrupt(NMI): It is the interrupt that cannot be masked or disabled by software
- Software Interrupt: It is an interrupt generated by the execution of Software interrupt instruction in 8086
- Trap interrupt: It is used for performing single-step operations in the 8086 and can be enabled or disabled using the T flag
- BHE: This is the BUS High Enable signal which is used to enable the upper bank of the memory in 8086

- Even/Low bank: The even/low bank is a memory chip that contains even memory addresses; its data lines are connected to the D7-D0 lines of 8086
- ODD/High bank: The ODD/High bank is a memory chip that contains odd memory addresses; its data lines are connected to the D15-D8 lines of 8086
- Memory Read control signal is activated during memory Read operation
- Memory Write control signal is activated during memory write operation

Communication Interface

- Simplex mode: Data is transmitted only in one direction over a single communication channel. For example, the processor may transmit data for a CRT display unit in this mode.
- Duplex Mode: In duplex mode, data may be transferred between two transreceivers in both directions simultaneously.
- Half Duplex mode: In this mode, data transmission may take place in either direction, but at a time data may be transmitted only in one direction. A computer may communicate with a terminal in this mode. It is not possible to transmit data from the computer to the terminal and terminal to computer simultaneously.
- Asynchronous Mode (Transmission): When a data character is sent to 8251A by the CPU, it adds start bits prior to the serial data bits, followed by optional parity bit and stop bits using the asynchronous mode instruction control word format. This sequence is then transmitted using TXD output pin on the falling edge of TXC.
- Asynchronous Mode (Receive): A falling edge on RXD input line marks a start bit. The receiver requires only one stop bit to mark end of the data bit string, regardless of the stop bit programmed at the transmitting end. The 8-bit character is then loaded into the into parallel I/O buffer of 8251.
- RXRDY pin is raised high to indicate to the CPU that a character is ready for it. If the previous character has not been read by the CPU, the new character replaces it, and the overrun flag is set indicating that the previous character is lost.
- Synchronous Mode (Transmission): The TXD output is high until the CPU sends a character to 8251 which usually is a SYNC character. When CTS line goes low, the first character is serially transmitted out. Characters are shifted out on the falling edge of TXC .Data is shifted out at the same rate as TXC , over TXD output line. If the CPU buffer becomes empty, the SYNC character or characters are inserted in the data stream over TXD output.
- Synchronous Mode (Receiver): In this mode, the character synchronization can be achieved internally or externally. The data on RXD pin is sampled on rising edge of the RXC. The content of the receiver buffer is compared with the first SYNC character at every edge until it matches. If 8251 is programmed for two SYNC characters, the subsequent received character is also checked.

- When the characters match, the hunting stops. The SYNDET pin set high and is reset automatically by a status read operation. In the external SYNC mode, the synchronization is achieved by applying a high level on the SYNDET input pin that forces 8251 out of HUNT mode. The high level can be removed after one RXC cycle. The parity and overrun error both are checked in the same way as in asynchronous mode.

Fill in the blanks / choose the Best:

1. While CPU is executing a program, an interrupt exists then it a) follows the next instruction in the program
b) jumps to instruction in other registers
c) **breaks the normal sequence of execution of instructions** d) stops executing the program

2. An interrupt breaks the execution of instructions and diverts its execution to a**)**
Interrupt service routine
b) Counter word register c) Execution unit
d) control unit

3. NMI stands for
a) **nonmaskable interrupt**
b) nonmultiple interrupt
c) nonmovable interrupt
d) none of the mentioned

4. If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called
a) maskable interrupt
b) **nonmaskable interrupt**
c) maskable interrupt and nonmaskable interrupt
d) none of the mentioned

5. The INTR interrupt may be a)
maskable
b) nonmaskable
c) maskable and nonmaskable d) none of the mentioned

6. The input and output operations are respectively similar to the operations
a) read, read
b) write, write
c) **read, write**
d) write, read

7. The operation, IOWR (active low) performs

a) write operation on input data
b) **write operation on output data**
c) read operation on input data
d) read operation on output data

8. The latch or IC 74LS373 acts as
a) good input port
b) bad input port
c) **good output port**
d) bad output port

9. In memory-mapped scheme, the devices are viewed as
a) distinct I/O devices
b) **memory locations**
c) only input devices
d) only output devices

10. Programmable peripheral input-output port is other name for
a) serial input-output port
b) **parallel input-output port**
c) serial input port
d) parallel output port

11. Port C of 8255 can function independently as
a) input port
b) output port
c) **either input or output ports**
d) both input and output ports

12. All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
a) data bus control

b) read logic control
c) **control word register**
d) none of the mentioned

13. The data bus buffer is controlled by
a) control word register
b) **read/write control logic**
c) data bus
d) none of the mentioned

14. The port that is used for the generation of handshake lines in mode 1 or mode 2 is a) port A

b) port B
c) port C Lower
d) **port C Upper**

15. If A1=0, A0=1 then the input read cycle is performed from
a) port A to data bus
b) **port B to data bus**
c) port C to data bus
d) CWR to data bus

16. Which of the following is not a mode of data transmission?
a) simplex
b) duplex
c) **semi duplex**
d) half duplex

17. In 8251A, the pin that controls the rate at which the character is to be transmitted is a)
TXC(active low)
b) TXC(active high)
c) TXD(active low)
d) RXC(active low)

18. TXD(Transmitted Data Output) pin carries serial stream of the transmitted data bits along with
a) start bit
b) stop bit
c) parity bit
d) **all of the mentioned**

19. The signal that may be used either to interrupt the CPU or polled by the CPU is
a) TXRDY(Transmitter ready)
b) **RXRDY(Receiver ready output)**
c) DSR(active low)
d) DTR(active low)

20. The disadvantage of RS-232C is a)
limited speed of communication b) high-
voltage level signaling
c) big-size communication adapters
d) **all of the mentioned**

UNIT-IV-ARM ARCHITECTURE

ARM Processor fundamentals, ARM Architecture – Register, CPSR, Pipeline, exceptions and interrupts interrupt vector table, ARM instruction set – Data processing, Branch instructions, load store instructions, Software interrupt instructions, Program status register instructions, loading constants, Conditional execution, Introduction to Thumb instructions.

SHORT QUESTIONS

1.What are the advantages of ARM controller?

2.what is register .how many types the ARM registers.

3.what are the interrupt vector register.

4.write the pipe lining concept.

5.what are the soft ware interrupts.

Long Questions

1.draw and explain the ARM architecture.

2.draw the architecture of CPSR.

3. Explain the Thumb instruction sets.

4.Explain the program instruction set.

Multiple Questions

1. Most of processors designed by ARM are

A. 16 bit
B. 32 bit
C. 64 bit
D. 8 bit

2. When clock capacitance is reduced, it

A. increases clock hold time
B. decreases clock hold time
C. changes datapath D.None

3. DMA controllers stands for

A. Direct Memory Alternation Controller
B. Direct Memory Access Controller
C. Direct Multi Access Controller
D. Double Memory Access Controller

4. A programmable timer device used to ensure that processor is running program is

A. Real Time Clock
B. Phase Lock Loop
C. Watchdog Timer
D. Simulation Time Clock

5. Fluctuation in power supply levels will produced due to

A. high di/dt
B. low di/dt
C. no di/dt
D. infinite di/dt

6. In microcontrollers, I2C stands for

A. Inter-Integrated Clock
B. Initial-Integrated Clock
C. Intel-Integrated Circuit
D. Inter-Integrated Circuit

7. Number of interrupts present in Cortex-M1 processors are

A. 1 to 32
B. 1 to 16
C. 1,8,16,32
D. 1 to 240

8. A serial data communication interface in microcontroller specifically used for audio information is

A. I2C

B. I2S
C. UART
D. GPIO

9. Cortex-R Processor consists of

A. cache memory
B. MPU
C. MMU
D. NVIC

10. Processor used in high performance power microcontrollers are

A. Cortex-M0 processor
B. Cortex-M3 processor
C. Cortex-M1 processor
D. Cortex-M7 processor